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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,302	10/27/2003	Douglas Vincent Larson	200309576-1	3575

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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,302	LARSON ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1 and 7-8 are rejected under U.S.C. 102(a) as being anticipated by Chavarria-Miranda et al. in the paper "An Evaluation of Data-Parallel Compiler Supporter for Line-Sweep Applications" (hereinafter, "Chavarria-Miranda").

Claim 1. A method of dynamically allocating memory when a program requests allocation of a memory block from a memory pool comprising steps of: *(Section 6.4, lines 1-2 – State that this is a method of dynamic memory allocation)*

- determining a spacer size; *(Section 7, lines 19-20 – State that the pads (spacers) are of an odd length. In other words, a size had to be determined)*
- reserving a spacer block of memory from the memory pool, the spacer block being of the spacer size; *(Section 6.4, lines 2-5 – State that each processor allocates memory)*
- and allocating the memory block, adjacent to the spacer block, from the memory pool. *(Section 7, Figure 20 – Shows how the memory block is adjacent to the spacer block)*

Claim 7. A computer program product comprising a computer readable media having recorded therein computer readable code for allocating memory, the computer readable code comprising computer readable code for executing steps of: *(Section 7, lines 13-18 – State that Fortran is utilized in a computer)*

- determining a spacer size; *(Section 7, lines 19-20 – State that the pads (spacers) are of an odd length. In other words, a size had to be determined)*
- reserving a spacer block of memory from a memory pool, the spacer block being of the spacer size; *(Section 6.4, lines 2-5 – State that each processor allocates memory)*

- and allocating a memory block of a requested size from the memory pool at a location adjacent to the spacer block. *(Section 7, Figure 20 – Shows how the memory block is adjacent to the spacer block)*

Claim 8. A computer system comprising:

- a processor; *(Section 7, lines 16-17 – State that the tiles are located on a processor)*
- a cache memory coupled to provide instructions and data to the processor; *(Section 7, lines 16-18 – State that the cache memory is coupled to the processor)*
- a memory system coupled to provide instructions and data to the cache memory upon the processor initiating memory access operations that miss in the cache; *(Section 6, lines 4-8)*
- wherein the memory system contains a dynamic memory allocation module for allocating memory from a pool of dynamically allocable memory upon memory allocation requests made by a program, and wherein the dynamic memory allocation module comprises computer readable code for avoiding cache thrashing by performing steps when memory allocation is requested by the program comprising: *(Section 6, lines 4-9 – Disclose the padded dynamically allocated arrays as well as the generated code)*
- determining a spacer size to reduce a likelihood of multiple hot spots in allocated memory blocks aligning in the same sets of cache; *(Section 7, lines 19-20 – State that the pads (spacers) are of an odd length and are used to minimize intra-array cache conflicts. In other words, a size had to be determined)*
- reserving a spacer block of memory from the memory pool, the spacer block being of the spacer size; *(Section 6.4, lines 2-5 – State that each processor allocates memory)*
- and allocating the memory block from the memory pool at a location in the pool adjacent to the spacer block. *(Section 7, Figure 20 – Shows how the memory block is adjacent to the spacer block)*

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 and 5-6 are rejected under 35 U.S.C.103(a) as being unpatentable over Chavarria-Miranda et al. as applied to claim 1 above, further in view of Cray T3E Fortran Optimization Guide (hereinafter "Cray"). .

Chavarria-Miranda teaches the limitations of claim 1 for the reasons above.

5. Chavarria-Miranda's invention differs from the claimed invention in that there is no specific mention of memory block reservation due to an exceeding of a memory-block limit.

Chavarria-Miranda fails to teach claim 2, which states "The method of claim 1, wherein the spacer block is reserved only if a previously allocated memory block exceeds a predetermined threshold size." However, Cray discloses the following: "For smaller arrays, between 128 and 1,023 words, it adds 8 words to reduce data cache and secondary cache conflict. Arrays with fewer than 128 words are not padded." (Section 4.3.3, lines 11-12). Therefore, Cray clearly states that padding does not take place unless the arrays have over 128 words, which denotes a pre-determined threshold size.

It would have been obvious to one of ordinary skill in the art, having the teachings of Chavarria-Miranda et al. and Cray et al. before him at the time the method was made, to design a method that had a pre-determined boundary that would allow for a spacer block (pad) to be created as taught by the dynamic allocation method of Cray, in Chavarria-Miranda's dynamic allocation method so as to save memory space and avoid congestion (cache thrashing), as taught by Cray.

6. Chavarria-Miranda's invention differs from the claimed invention in that there is no specific mention of random spacer size creation within a specific boundary.

Chavarria-Miranda fails to teach claim 5, which states "The method of claim 1, wherein

the step of determining a spacer size generates a random spacer size within a predetermined range of allowable spacer size." However, Cray discloses the following: "For large arrays of 1,024 words or more, it adds up to 264 words of padding for every 4,096 words in the array to reduce secondary cache conflict." (Section 4.3.3, lines 7-8). By Cray stating that there are "up to 264 words of padding" he is declaring that there are random spacer sizes.

It would have been obvious to one of ordinary skill in the art, having the teachings of Chavarria-Miranda et al. and Cray et al. before him at the time the method was made, to design a method that determined a random spacer size within a particular allowable range as taught by the dynamic allocation method of Cray, in Chavarria-Miranda's dynamic allocation method so as to save memory space and avoid congestion (cache thrashing), as taught by Cray.

7. Chavarria-Miranda's invention differs from the claimed invention in that there is no specific mention of how to determine the addition of spacer size.

Chavarria-Miranda fails to teach claim 6, which states "The method of claim 1, wherein the step of determining a spacer size operates according to a block's allocated count." However, Cray discloses the following: "Using the first option, the compiler adds padding that depends on the size of the array". (Section 4.3.3, line 6). Cray also discloses the following: "For large arrays of 1,024 words or more, it adds up to 264 words of padding for every 4,096 words in the array to reduce secondary cache conflict." (Section 4.3.3, lines 7-8).

It would have been obvious to one of ordinary skill in the art, having the teachings of Chavarria-Miranda et al. and Cray et al. before him at the time the method was made, to design a method that determined a spacer size according to a memory block's allocated count as taught by the dynamic allocation method of Cray, in Chavarria-Miranda's dynamic allocation method so as

to save memory space and avoid congestion (cache thrashing), as taught by Cray.

8. Claim 3 is rejected under 35 U.S.C.103(a) as being unpatentable over Chavarria-Miranda as applied to claims 1 and 2 above.

Chavarria-Miranda teaches the limitations of claims 1 and 2 for the reasons above.

Chavarria-Miranda's invention differs from the claimed invention in that there is no specific reference to the reservation of a memory block only if it is of a particular size.

Chavarria-Miranda fails to teach claim 3, which states "The method of claim 2, wherein the spacer block is reserved only if a previously allocated memory block is of size divisible by a predetermined power of two." However, stating that the memory block needs to be of a size "divisible by two" does not change the purpose or functionality of the claimed "method of dynamically allocating memory". Therefore, it would have been obvious to one of ordinary skill in the art to declare the memory blocks of Chavarria-Miranda to be "divisible by two" so that the memory block begins at a location that is in even multiple of a page size, which is typically a power of two.

For further information, reference Gardner v. TEC Systems, Inc., which states "where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device".

9. Claim 4 is rejected under 35 U.S.C.103(a) as being unpatentable over Chavarria-Miranda as applied to claims 1-3 above.

Chavarria-Miranda teaches the limitations of claims 1-3 for the reasons above.

Chavarria-Miranda's invention differs from the claimed invention in that there is no specific reference to making the size and threshold of the memory block to be adjustable.

Chavarria-Miranda fails to teach claim 4, which states "The method of claim 3, wherein the predetermined power of two and the predetermined threshold size are parameterized such that they may be adjusted to optimize performance." However, stating that the memory block size and threshold may be adjustable does not change the purpose or functionality of the claimed "method of dynamically allocating memory". Therefore, it would have been obvious to one of ordinary skill in the art to declare the memory blocks of Chavarria-Miranda to be adjustable so that performance may be optimized.

For further information, reference Stevens (212 F.2d 197, 101 USPQ 284 (CCPA 1954)), which states the following: "The court held that adjustability, where needed, is not a patentable advance..."

10. Claim 9 is rejected under 35 U.S.C.103(a) as being unpatentable over Chavarria-Miranda et al. as applied to claim 8 above, further in view of Cray et al. (Documentation).

Chavarria-Miranda teaches the limitations of claim 8 for the reasons above.

Chavarria-Miranda fails to teach claim 9, which states "The computer system of claim 8 wherein the spacer size is determined by randomly selecting a spacer size such the spacer size is in a range of permissible spacer sizes." However, Cray discloses the following: "For large arrays of 1,024 words or more, it adds up to 264 words of padding for every 4,096 words in the array to reduce secondary cache conflict." (Section 4.3.3, lines 7-8).

It would have been obvious to one of ordinary skill in the art, having the teachings of

Chavarria-Miranda et al. and Cray et al. before him at the time the method was made, to design a Computer system that determined a random spacer size within a particular allowable range as taught by the Computer system of Cray, in Chavarria-Miranda's computer system method so as to save memory space and avoid congestion (cache thrashing), as taught by Cray.

11. Claim 10 is rejected under 35 U.S.C.103(a) as being unpatentable over Chavarria-Miranda as applied to claims 8-9 above.

Chavarria-Miranda teaches the limitations of claims 8-9 for the reasons above.

Chavarria-Miranda's invention differs from the claimed invention in that there is no specific reference to making the spacer size adjustable by an administrator.

Chavarria-Miranda fails to teach claim 10, which states "The computer system of claim wherein the range of permissible spacer sizes is adjustable by a system administrator." However, stating that the spacer size may be adjustable by an administrator does not change the purpose or functionality of the claimed "computer system". Therefore, it would have been obvious to one of ordinary skill in the art to declare the spacer sizes of Chavarria-Miranda to be adjustable by an administrator so that performance may be optimized.

For further information, reference Stevens (212 F.2d 197, 101 USPQ 284 (CCPA 1954)), which states the following: "The court held that adjustability, where needed, is not a patentable advance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER